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IN THE CLAIMS*The status of the claims as presently amended is as follows:*

1-33. (Canceled)

34. (Currently Amended) ~~A~~The semiconductor device comprising:

- ~~— a semiconductor chip;~~
- ~~— a layer with low electrical resistance of a first conductivity type or a second conductivity type in the bottom portion of the semiconductor chip;~~
- ~~— a breakdown voltage sustaining layer above the layer with low electrical resistance, the breakdown voltage sustaining layer comprising at least one or more semiconductor regions of the first conductivity type;~~
- ~~— a well region of the second conductivity type in the surface portion of the breakdown voltage sustaining layer; and~~
- ~~— guard rings of the second conductivity type in the surface portion of the semiconductor chip, the guard rings surrounding the well region;~~
- ~~— according to claim 37, wherein the number of the guard rings is equal to or more than the number n calculated by the following equation, the expression $n = 1.0 \text{ or greater} \times V_{br}/100$; and,~~ wherein V_{br} (V) is the breakdown voltage of the semiconductor device.

35. (Currently Amended) The semiconductor device according to Claim 34, wherein the number of the guard rings is equal to or more than the number n calculated by the following equation, expression $n = 1.5 \times V_{br}/100$.

36. (Currently Amended) The semiconductor device according to Claim 34, wherein the number of the guard rings is equal to or less than the number n calculated by the following equation, expression $n = 6.0 \times V_{br}/100$.

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37. *(Original)* A semiconductor device comprising:

a semiconductor chip;

a layer with low electrical resistance of a first conductivity type or a second conductivity type in the bottom portion of the semiconductor chip;

a breakdown-voltage sustaining layer above the layer with low electrical resistance, the breakdown-voltage sustaining layer comprising at least one or more semiconductor regions of the first conductivity type;

a well region of the second conductivity type in the surface portion of the breakdown-voltage sustaining layer;

guard rings of the second conductivity type in the surface portion of the semiconductor chip, the guard rings surrounding the well region; and

wherein the spacing between the well region and the first guard ring nearest to the well region being 1 μm or less.

38. *(Canceled)*

39. *(Currently Amended)* The semiconductor device according to Claim 37, wherein the spacing between the well region and the first guard ring is 0.5 μm or less[[r]].

40. *(Currently Amended)* The semiconductor device according to Claim [[38]]34, wherein the spacing between the well region and the first guard ring is 0.5 μm or less.

41. *(Original)* The semiconductor device according to Claim 39, wherein the first guard ring is in contact with the well region.

42. *(Original)* The semiconductor device according to Claim 40, wherein the first guard ring is in contact with the well region.

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43. *(Original)* The semiconductor device according to Claim 37, wherein the spacing between the first guard ring and the second guard ring second nearest to the well region is 1.5 μm or less.

44. *(Currently Amended)* The semiconductor device according to Claim ~~[[38]]~~34, wherein the spacing between the first guard ring and the second guard ring second nearest to the well region is 1.5 μm or less.

45. *(Original)* The semiconductor device according to Claim 43, wherein the spacing between the first guard ring and the second guard is 1 μm or less.

46. *(Currently Amended)* The semiconductor device according to Claim 44, wherein the spacing between the first guard ring and the second guard is 1 μm or less~~[[r]]~~.

47. *(Original)* The semiconductor device according to Claim 45, wherein the spacing between the first guard ring and the second guard ring is 0.5 μm or less.

48. *(Original)* The semiconductor device according to Claim 46, wherein the spacing between the first guard ring and the second guard ring is 0.5 μm or less.

49. *(Original)* The semiconductor device according to Claim 43, wherein the spacing between the second guard ring and the third guard ring third nearest to the well region is 2.0 μm or less.

50. *(Original)* The semiconductor device according to Claim 44, wherein the spacing between the second guard ring and the third guard ring third nearest to the well region is 2.0 μm or less.

51. *(Original)* The semiconductor device according to Claim 49, wherein the spacing between the second guard ring and the third guard ring is 1.0 μm or less.

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52. *(Original)* The semiconductor device according to Claim 50, wherein the spacing between the second guard ring and the third guard ring is 1.0 μm or less.

53. *(Original)* The semiconductor device according to Claim 49, wherein the spacing between the third guard ring and the fourth guard ring fourth nearest to the well region is 2.5 μm or less.

54. *(Original)* The semiconductor device according to Claim 50, wherein the spacing between the third guard ring and the fourth guard ring fourth nearest to the well region is 2.5 μm or less.

55. *(Original)* The semiconductor device according to Claim 53, wherein the spacing between the third guard ring and the fourth guard ring is 2.0 μm or less.

56. *(Original)* The semiconductor device according to Claim 54, wherein the spacing between the third guard ring and the fourth guard ring is 2.0 μm or less.

57. *(Original)* A semiconductor device comprising:

- a semiconductor chip;

- a layer with low electrical resistance of a first conductivity type or a second conductivity type in the bottom portion of the semiconductor chip;

- a breakdown-voltage sustaining layer above the layer with low electrical resistance, the breakdown-voltage sustaining layer comprising at least one or more semiconductor regions of the first conductivity type;

- a well region of the second conductivity type in the surface portion of the breakdown-voltage sustaining layer;

- guard rings of the second conductivity type in the surface portion of the semiconductor chip, the guard rings surrounding the well region; and

- wherein the spacing between the well region and the first guard ring nearest to the well region being $d_1/4$ or less, said d_1 being a shallower one of the junction depth of the well region

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and the junction depth of the guard rings.

58. (*Currently Amended*) The semiconductor device according to Claim ~~[[34]]~~57, wherein the spacing between the well region and the first guard ring nearest to the well region is $d_1/4$ or less, where said d_1 is a shallower one of the junction depth of the well region and the junction depth of the guard rings the number of the guard rings is equal to or more than the number n calculated by an expression $n = 1.0 \times V_{br}/100$, where V_{br} (V) is the breakdown voltage of the semiconductor device.

59. (*Original*) The semiconductor device according to Claim 57, wherein the spacing between the well region and the first guard ring is $d_1/8$ or less.

60. (*Original*) The semiconductor device according to Claim 58, wherein the spacing between the well region and the first guard ring is $d_1/8$ or less.

61. (*Original*) The semiconductor device according to Claim 57, wherein the spacing between the first guard ring and the second guard ring second nearest to the well region is $d_2/4$ or less, where said d_2 is the junction depth of the guard rings.

62. (*Original*) The semiconductor device according to Claim 58, wherein the spacing between the first guard ring and the second guard ring second nearest to the well region is $d_2/4$ or less, where said d_2 is the junction depth of the guard rings.

63. (*Original*) The semiconductor device according to Claim 61, wherein the spacing between the first guard ring and the second guard ring is $d_2/8$ or less.

64. (*Original*) The semiconductor device according to Claim 62, wherein the spacing between the first guard ring and the second guard ring is $d_2/8$ or less.

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65. *(Original)* The semiconductor device according to Claim 61, wherein the spacing between the second guard ring and the third guard ring third nearest to the well region is $d_2/4$ or less.

66. *(Original)* The semiconductor device according to Claim 62, wherein the spacing between the second guard ring and the third guard ring third nearest to the well region is $d_2/4$ or less.

67. *(Original)* The semiconductor device according to Claim 65, wherein the spacing between the second guard ring and the third guard ring is $d_2/8$ or less.

68. *(Original)* The semiconductor device according to Claim 66, wherein the spacing between the second guard ring and the third guard ring is $d_2/8$ or less.

69. *(Original)* The semiconductor device according to Claim 34, wherein the difference $I_2 - I_1$ between the spacing I_2 between the first guard ring nearest to the well region and the second guard ring second nearest to the well region and the spacing I_1 between the well region and the first guard ring is $1\text{ }\mu\text{m}$ or less.

70. *(Original)* The semiconductor device according to Claim 37, wherein the difference $I_2 - I_1$ between the spacing I_2 between the first guard ring nearest to the well region and the second guard ring second nearest to the well region and the spacing I_1 between the well region and the first guard ring is $1\text{ }\mu\text{m}$ or less.

71. *(Original)* The semiconductor device according to Claim 57, wherein the difference $I_2 - I_1$ between the spacing I_2 between the first guard ring nearest to the well region and the second guard ring second nearest to the well region and the spacing I_1 between the well region and the first guard ring is $1\text{ }\mu\text{m}$ or less.

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72. (Currently Amended) ~~The~~ A semiconductor device according to Claim 69, comprising:

a semiconductor chip;

a layer with low electrical resistance of a first conductivity type or a second conductivity type in the bottom portion of the semiconductor chip;

a breakdown-voltage sustaining layer above the layer with low electrical resistance, the breakdown-voltage sustaining layer comprising at least one or more semiconductor regions of the first conductivity type;

a well region of the second conductivity type in the surface portion of the breakdown-voltage sustaining layer; and

guard rings of the second conductivity type in the surface portion of the semiconductor chip, the guard rings surrounding the well region.

wherein the difference $I_2 - I_1$ between the spacing I_2 between the first guard ring nearest to the well region and the second guard ring second nearest to the well region and the spacing I_1 between the well region and the first guard ring is from 0.2 to 0.8 μm .

73. (Original) The semiconductor device according to Claim 70, wherein the difference $I_2 - I_1$ is from 0.2 to 0.8 μm .

74. (Original) The semiconductor device according to Claim 71, wherein the difference $I_2 - I_1$ is from 0.2 to 0.8 μm .

75. (Original) The semiconductor device according to Claim 69, wherein the difference $I_3 - I_2$ between the spacing I_3 between the second guard ring and the third guard ring third nearest to the well region and the spacing I_2 between the first guard ring and the second guard ring is 1 μm or less.

76. (Original) The semiconductor device according to Claim 70, wherein the difference $I_3 - I_2$ between the spacing I_3 between the second guard ring and the third guard ring third nearest to the

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well region and the spacing I_2 between the first guard ring and the second guard ring is 1 μm or less.

77. (Original) The semiconductor device according to Claim 71, wherein the difference $I_3 - I_2$ between the spacing I_3 between the second guard ring and the third guard ring third nearest to the well region and the spacing I_2 between the first guard ring and the second guard ring is 1 μm or less.

78. (Currently Amended) ~~The~~ semiconductor device according to ~~Claim 75, comprising:~~

a semiconductor chip;

a layer with low electrical resistance of a first conductivity type or a second conductivity type in the bottom portion of the semiconductor chip;

a breakdown-voltage sustaining layer above the layer with low electrical resistance, the breakdown-voltage sustaining layer comprising at least one or more semiconductor regions of the first conductivity type;

a well region of the second conductivity type in the surface portion of the breakdown-voltage sustaining layer; and

guard rings of the second conductivity type in the surface portion of the semiconductor chip, the guard rings surrounding the well region.

wherein the difference $I_3 - I_2$ between the spacing I_3 between the second guard ring second nearest to the well region and the third guard ring third nearest to the well region and the spacing I_2 between the well region and the first guard ring nearest to the well region is from 0.2 to 0.8 μm .

79. (Original) The semiconductor device according to Claim 76, wherein the difference $I_3 - I_2$ is from 0.2 to 0.8 μm .

80. (Original) The semiconductor device according to Claim 77, wherein the difference $I_3 - I_2$ is

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from 0.2 to 0.8 μm .

81. *(Original)* The semiconductor device according to Claim 75, wherein the difference $I_4 - I_3$ between the spacing I_4 between the third guard ring and the fourth guard ring fourth nearest to the well region and the spacing I_3 between the second guard ring and the third guard ring is 1 μm or less.

82. *(Original)* The semiconductor device according to Claim 76, wherein the difference $I_4 - I_3$ between the spacing I_4 between the third guard ring and the fourth guard ring fourth nearest to the well region and the spacing I_3 between the second guard ring and the third guard ring is 1 μm or less.

83. *(Original)* The semiconductor device according to Claim 77, wherein the difference $I_4 - I_3$ between the spacing I_4 between the third guard ring and the fourth guard ring fourth nearest to the well region and the spacing I_3 between the second guard ring and the third guard ring is 1 μm or less.

84. *(Currently Amended)* ~~The~~ A semiconductor device according to Claim 81, comprising:

a semiconductor chip;

a layer with low electrical resistance of a first conductivity type or a second conductivity type in the bottom portion of the semiconductor chip;

a breakdown-voltage sustaining layer above the layer with low electrical resistance, the breakdown-voltage sustaining layer comprising at least one or more semiconductor regions of the first conductivity type;

a well region of the second conductivity type in the surface portion of the breakdown-voltage sustaining layer; and

guard rings of the second conductivity type in the surface portion of the semiconductor chip, the guard rings surrounding the well region.

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wherein the difference $I_4 - I_3$ between the spacing I_4 between the third guard ring third nearest to the well region and the fourth guard ring fourth nearest to the well region and the spacing I_3 between the second guard ring second nearest to the well region and the third guard ring is from 0.2 to 0.8 μm .

85. *(Original)* The semiconductor device according to Claim 82, wherein the difference $I_4 - I_3$ is from 0.2 to 0.8 μm .

86. *(Original)* The semiconductor device according to Claim 83, wherein the difference $I_4 - I_3$ is from 0.2 to 0.8 μm .

87. *(Original)* The semiconductor device according to Claim 34, wherein the number of the guard rings is five or more, and the width of the first guard ring nearest to the well region is wider than the width of the fifth guard ring fifth nearest to the well region.

88. *(Original)* The semiconductor device according to Claim 37, wherein the number of the guard rings is five or more, and the width of the first guard ring nearest to the well region is wider than the width of the fifth guard ring fifth nearest to the well region.

89. *(Original)* The semiconductor device according to Claim 57, wherein the number of the guard rings is five or more, and the width of the first guard ring nearest to the well region is wider than the width of the fifth guard ring fifth nearest to the well region.

90. *(Original)* The semiconductor device according to Claim 87, wherein the number of the guard rings is six or more, and the width of the second guard ring second nearest to the well region is wider than the width of the sixth guard ring sixth nearest to the well region.

91. *(Original)* The semiconductor device according to Claim 88, wherein the number of the

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guard rings is six or more, and the width of the second guard ring second nearest to the well region is wider than the width of the sixth guard ring sixth nearest to the well region.

92. *(Original)* The semiconductor device according to Claim 89, wherein the number of the guard rings is six or more, and the width of the second guard ring second nearest to the well region is wider than the width of the sixth guard ring sixth nearest to the well region.

93. *(Original)* The semiconductor device according to Claim 90, wherein the number of the guard rings is seven or more, and the width of the third guard ring third nearest to the well region is wider than the width of the seventh guard ring seventh nearest to the well region.

94. *(Original)* The semiconductor device according to Claim 91, wherein the number of the guard rings is seven or more, and the width of the third guard ring third nearest to the well region is wider than the width of the seventh guard ring seventh nearest to the well region.

95. *(Original)* The semiconductor device according to Claim 92, wherein the number of the guard rings is seven or more, and the width of the third guard ring third nearest to the well region is wider than the width of the seventh guard ring seventh nearest to the well region.

96. *(Withdrawn)* The semiconductor device according to Claim 34, further comprising an electrical conductor film above the surface of the breakdown-voltage sustaining layer between the well region and the first guard ring nearest to the well region with an insulation film interposed between the electrical conductor film and the surface of the breakdown-voltage sustaining layer.

97. *(Withdrawn)* The semiconductor device according to Claim 37, further comprising an electrical conductor film above the surface of the breakdown-voltage sustaining layer between the well region and the first guard ring nearest to the well region with an insulation film

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interposed between the electrical conductor film and the surface of the breakdown-voltage sustaining layer.

98. (*Withdrawn*) The semiconductor device according to Claim 57, further comprising an electrical conductor film above the surface of the breakdown-voltage sustaining layer between the well region and the first guard ring nearest to the well region with an insulation film interposed between the electrical conductor film and the surface of the breakdown-voltage sustaining layer.

99. (*Withdrawn*) The semiconductor device according to Claim 96, further comprising an electrical conductor film above the surface of the breakdown-voltage sustaining layer between the first guard ring and the second guard ring second nearest to the well region with an insulation film interposed between the electrical conductor film and the surface of the breakdown-voltage sustaining layer.

100. (*Withdrawn*) The semiconductor device according to Claim 97, further comprising an electrical conductor film above the surface of the breakdown-voltage sustaining layer between the first guard ring and the second guard ring second nearest to the well region with an insulation film interposed between the electrical conductor film and the surface of the breakdown-voltage sustaining layer.

101. (*Withdrawn*) The semiconductor device according to Claim 98, further comprising an electrical conductor film above the surface of the breakdown-voltage sustaining layer between the first guard ring and the second guard ring second nearest to the well region with an insulation film interposed between the electrical conductor film and the surface of the breakdown-voltage sustaining layer.

102. (*Withdrawn*) The semiconductor device according to Claim 99, wherein the number n of

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the guard rings is three or more and the semiconductor device further comprises an electrical conductor film above the surface of the breakdown-voltage sustaining layer between the second guard ring and the third guard ring third nearest to the well region with an insulation film interposed between the electrical conductor film and the surface of the breakdown-voltage sustaining layer.

103. (*Withdrawn*) The semiconductor device according to Claim 100, wherein the number n of the guard rings is three or more and the semiconductor device further comprises an electrical conductor film above the surface of the breakdown-voltage sustaining layer between the second guard ring and the third guard ring third nearest to the well region with an insulation film interposed between the electrical conductor film and the surface of the breakdown-voltage sustaining layer.

104. (*Withdrawn*) The semiconductor device according to Claim 101, wherein the number n of the guard rings is three or more and the semiconductor device further comprises an electrical conductor film above the surface of the breakdown-voltage sustaining layer between the second guard ring and the third guard ring third nearest to the well region with an insulation film interposed between the electrical conductor film and the surface of the breakdown-voltage sustaining layer.

105. (*Withdrawn*) The semiconductor device according to Claim 102, wherein the number n of the guard rings is four or more and the semiconductor device further comprises an electrical conductor film above the surface of the breakdown-voltage sustaining layer between the third guard ring and the fourth guard ring fourth nearest to the well region with an insulation film interposed between the electrical conductor film and the surface of the breakdown-voltage sustaining layer.

106. (*Withdrawn*) The semiconductor device according to Claim 103, wherein the number n of

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the guard rings is four or more and the semiconductor device further comprises an electrical conductor film above the surface of the breakdown-voltage sustaining layer between the third guard ring and the fourth guard ring fourth nearest to the well region with an insulation film interposed between the electrical conductor film and the surface of the breakdown-voltage sustaining layer.

107. *(Withdrawn)* The semiconductor device according to Claim 104, wherein the number n of the guard rings is four or more and the semiconductor device further comprises an electrical conductor film above the surface of the breakdown-voltage sustaining layer between the third guard ring and the fourth guard ring fourth nearest to the well region with an insulation film interposed between the electrical conductor film and the surface of the breakdown-voltage sustaining layer.

108. *(Withdrawn)* The semiconductor device according to Claim 96, wherein the electrical conductor film is at a floating potential.

109. *(Withdrawn)* The semiconductor device according to Claim 97, wherein the electrical conductor film is at a floating potential.

110. *(Withdrawn)* The semiconductor device according to Claim 98, wherein the electrical conductor film is at a floating potential.

111. *(Withdrawn)* The semiconductor device according to Claim 34, wherein the breakdown-voltage sustaining layer comprises semiconductor regions of the first conductivity type and semiconductor regions of the second conductivity type arranged alternately.

112. *(Withdrawn)* The semiconductor device according to Claim 37, wherein the breakdown-voltage sustaining layer comprises semiconductor regions of the first conductivity type and

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semiconductor regions of the second conductivity type arranged alternately.

113. (*Withdrawn*) The semiconductor device according to Claim 57, wherein the breakdown-voltage sustaining layer comprises semiconductor regions of the first conductivity type and semiconductor regions of the second conductivity type arranged alternately.

114-115. (*Canceled*)

116. (*Withdrawn*) The semiconductor device according to Claim 34, further comprising an organic polymer film protecting the surface of the semiconductor device.

117. (*Withdrawn*) The semiconductor device according to Claim 37, further comprising an organic polymer film protecting the surface of the semiconductor device.

118. (*Withdrawn*) The semiconductor device according to Claim 57, further comprising an organic polymer film protecting the surface of the semiconductor device.